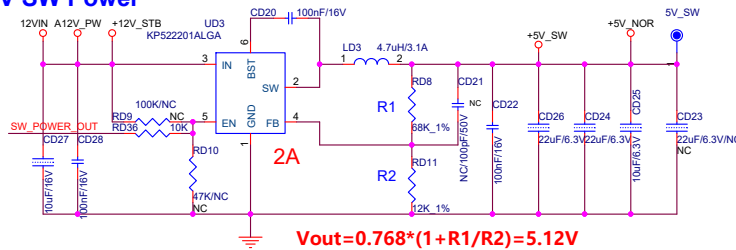
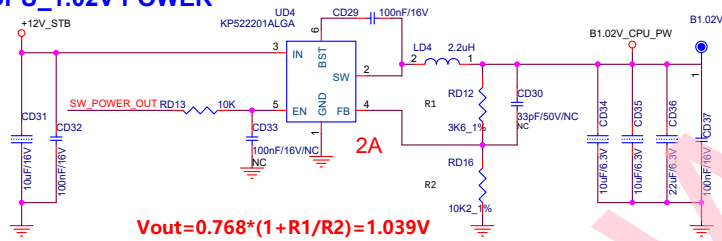


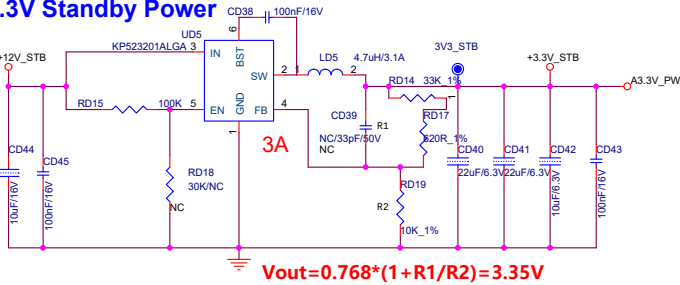
5V SW Power



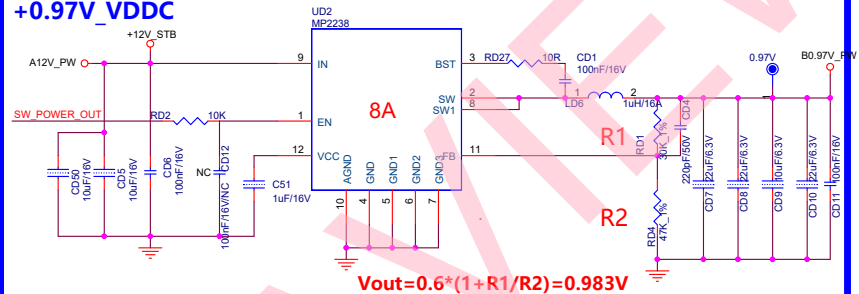
CPU_1.02V POWER



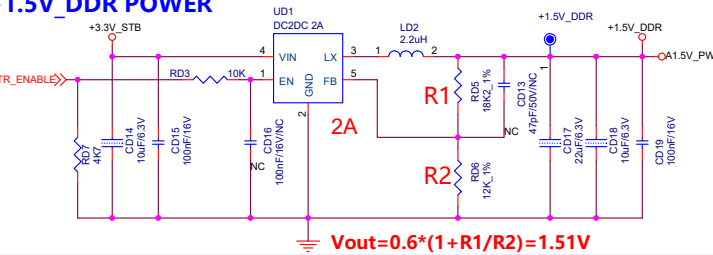
3.3V Standby Power



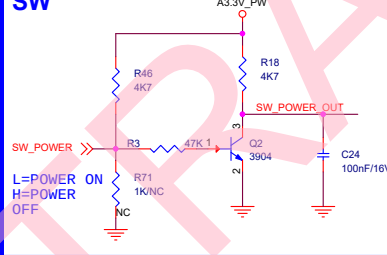
+0.97V_VDDC



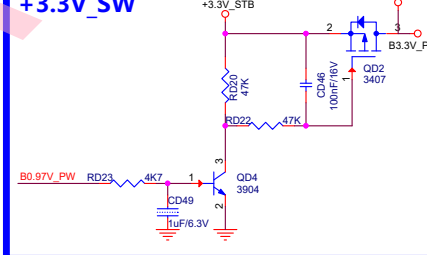
+1.5V_DDR POWER



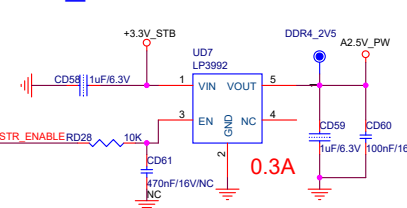
SW



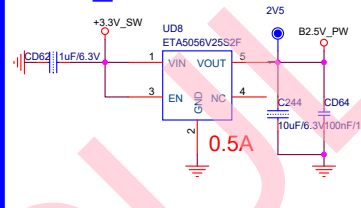
+3.3V_SW



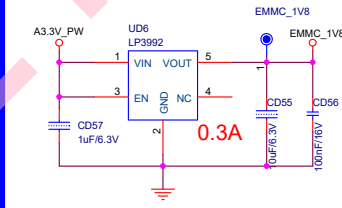
DDR4_2.5V



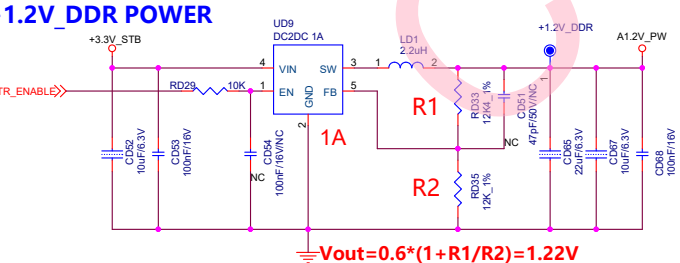
MAIN_2.5V

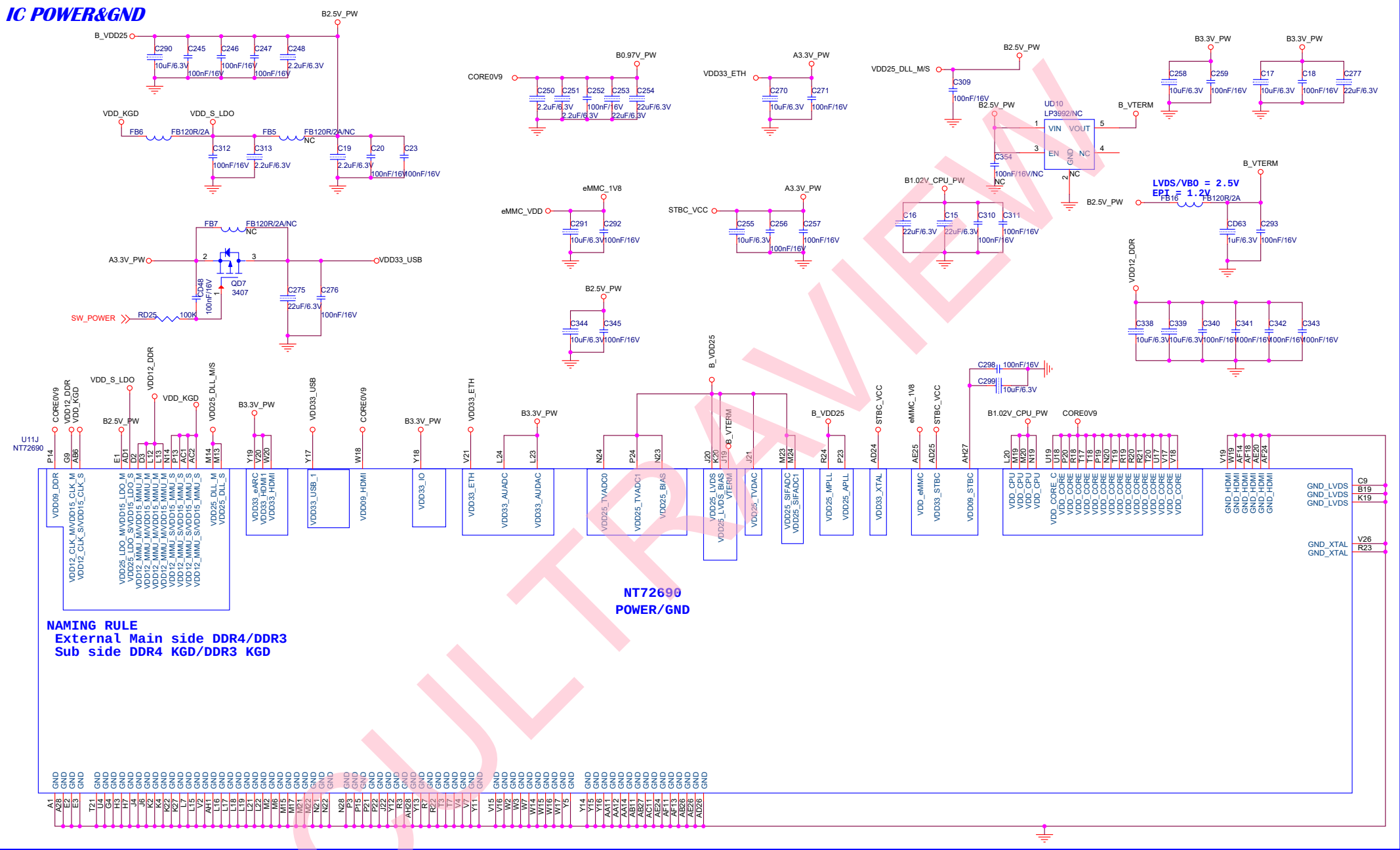


EMMC 1.8V



+1.2V_DDR POWER



IC POWER&GND

NAMING RULE
External Main side DDR4/DDR3
Sub side DDR4 KGD/DDR3 KGD

[illegible][illegible][illegible]

J10

21	DATA2+	1	RXD2+
21	DATA2_SHIELD	2	
21	DATA2-	3	RXD2-
21	DATA1+	4	RXD1+
21	DATA1_SHIELD	5	
21	DATA1-	6	RXD1-
22	DAT1A+	7	RXD0+
22	DAT1A_SHIELD	8	
22	DAT1A-	9	RXD0-
22	DATA0+	10	RXD0+
22	DATA0_SHIELD	11	
22	DATA0-	12	RXD0-
23	CLK+	13	CEC
23	CLK_SHIELD	14	H eARC+
23	CLK-	15	HDMID SCL
23	NC	16	HDMID SDA
23	SCL	17	
23	SDA	18	
20	CEC GND	19	HPD D/eARC-
20	+5V POWER		
20	HOT PLUG		

HDMI

U19 ESB-CS0806S/NC NC

10	RXDC-	1	RXDC-
9	RXDC+	2	RXDC+
8		3	
7	RXD0-	4	RXD0-
6	RXD0+	5	RXD0+
		S4	

U19 ESB-CS0806S/NC NC

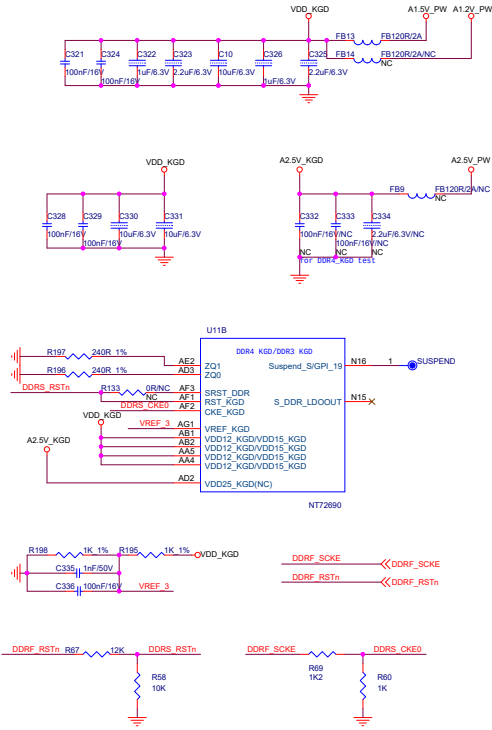
10	RXD1-	1	RXD1-
9	RXD1+	2	RXD1+
8		S6	
7	RXD2-	3	RXD2-
6	RXD2+	4	RXD2+
		S7	
		S8	

Components and Connections:

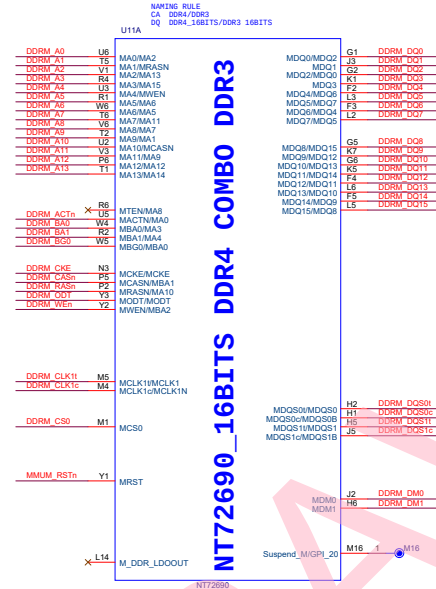
- C6:** 1pF/50V/NC, connected between J10 pin 11 and NC.
- R112:** 47K, connected between J10 pin 15 and R115.
- R111:** 47K, connected between J10 pin 16 and R115.
- C5:** 1pF/50V/NC, connected between J10 pin 19 and GND.
- R115:** 4K7, connected between the HDMI signal line and PWR5V_D.
- R335:** 10K, connected between the HDMI signal line and GND.

[illegible][illegible]

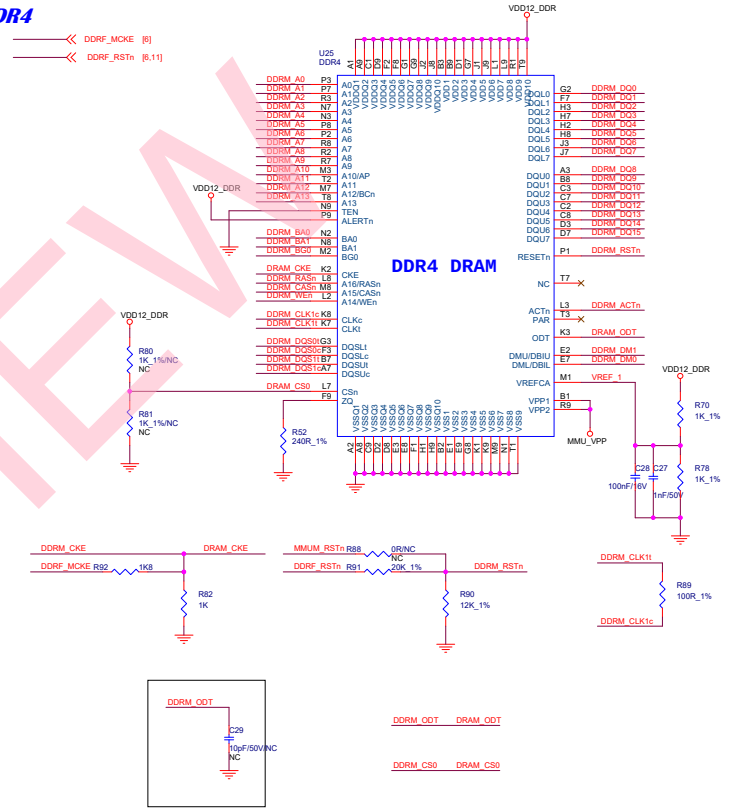
DDR_S



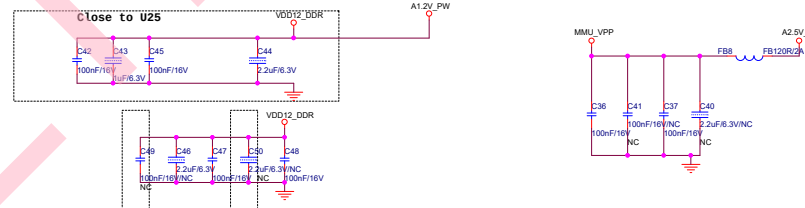
DDR_M

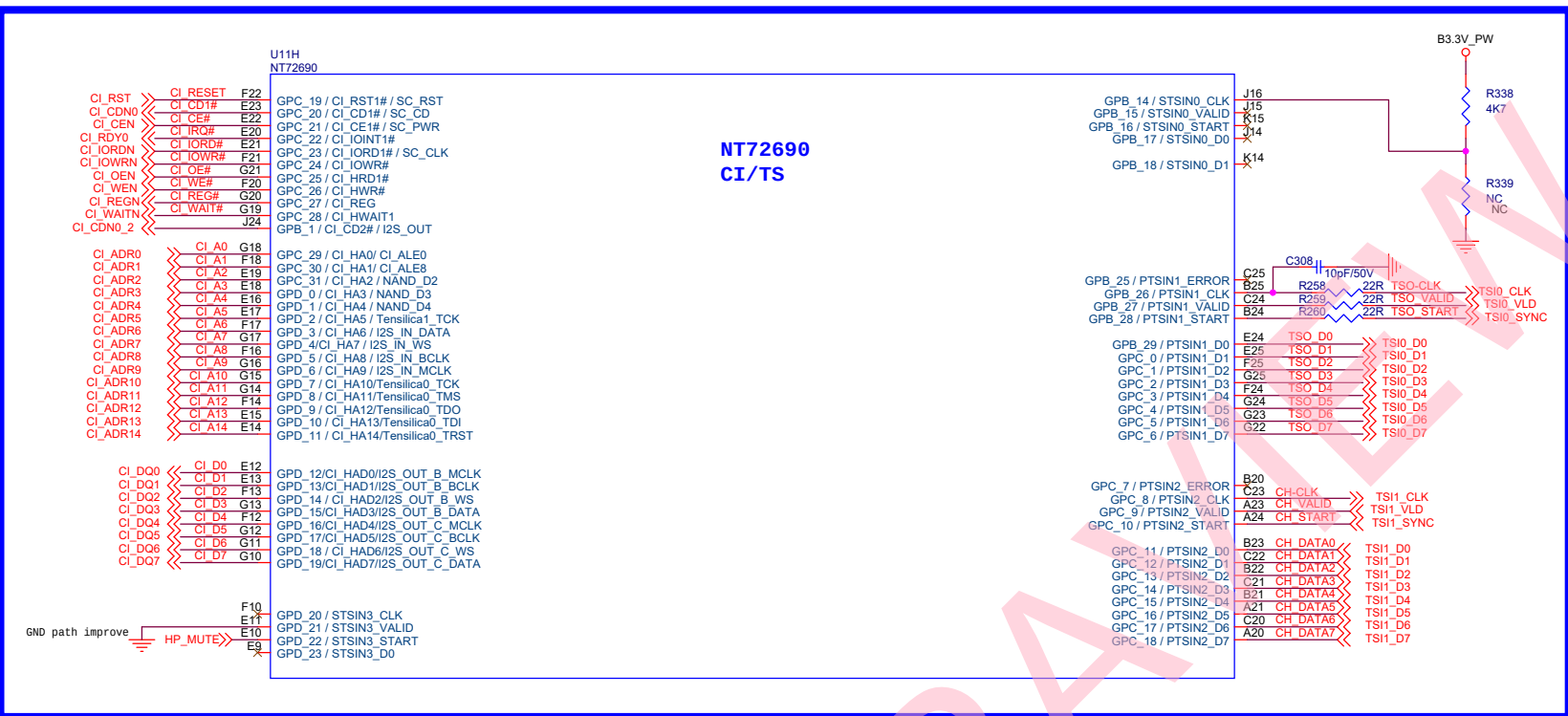


DDR4



DDR4_POWER





CPU Side:

BS0_Bypass CPU MaskROM
0 : Using CPU MaskROM
1 : Bypass CPU MaskROM

eMMC:

BS13_eMMC bus width
BS13 =
0: EMMC Bus width is 8 bit
1: EMMC Bus width is 4 bit

BS15_eMMC ACK
0: Boot mode wait ACK
1: Boot mode do not wait ACK

BS18_eMMC clk_switch
0: 26M
1: 13M

STBC Side:

BS1_STBC Boot Strap Option
0: Boot from STBC
1: Boot from CPU, bypass STBC.

BS8_STBC watchdog
0: Default disable STBC watchdog
1: Default enable STBC watchdog

BS19_Internal boot strap for NF/eMMC type
0: NF/eMMC type internal boot strap enable
1: NF/eMMC type internal boot strap disable
(BS[7:6] = 00, BS8 is external; BS[17:16]=00, BS14=0, BS13, BS15, BS18 are external)

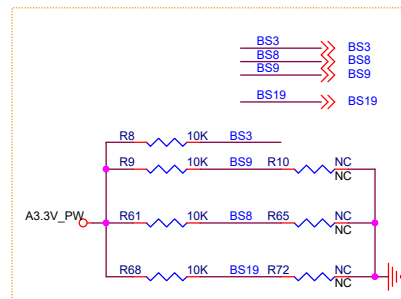
BS9_Security boot
0: no security boot
1: security boot

BS20_NAND I/O
0: NAND I/O in STBC eMMC side (BS12 = 1)
1: NAND I/O in ARM CI side (BS12 = 1, BS[4:3] = 00, 11)
or STBC SPI side (BS12 = 1, BS[4:3] = 01, 10)

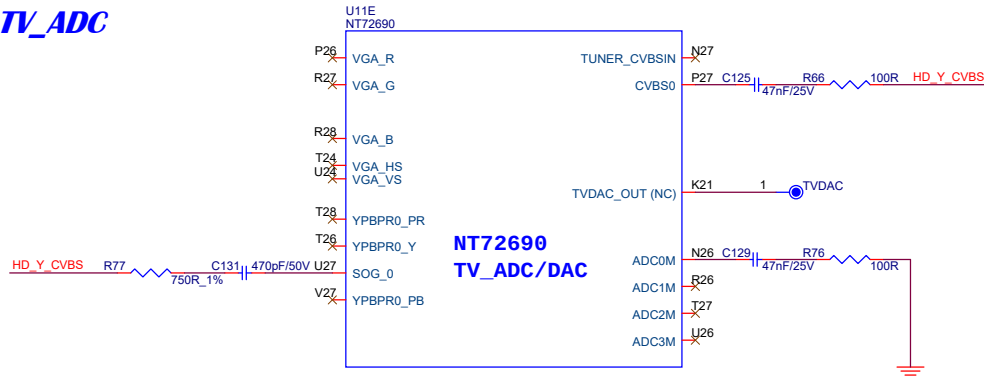
BS2_Bypass STBC MaskROM
When BS1=0,
0: Through STBC MaskROM
1: Bypass STBC MaskROM

BS10_SPI Flash scramble
0: Disable
1: Enable
BS11_Turnkey Security
0: Disable
1: Enable

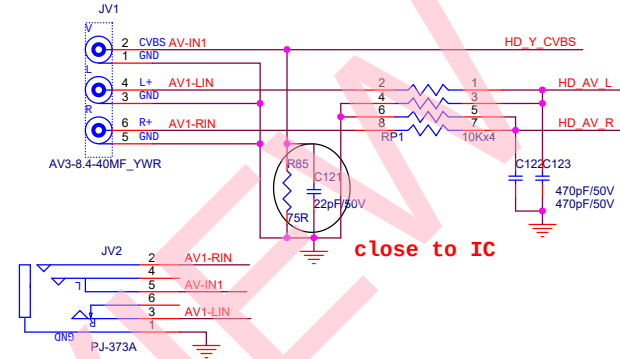
BS12=0 , BS3,BS4_Device
BS4, 3 =
00: STBC boot from SPI, CPU boot from eMMC
01: STBC & CPU both boot from eMMC
10: STBC & CPU both boot from SPI
11: Reserved (same 00)



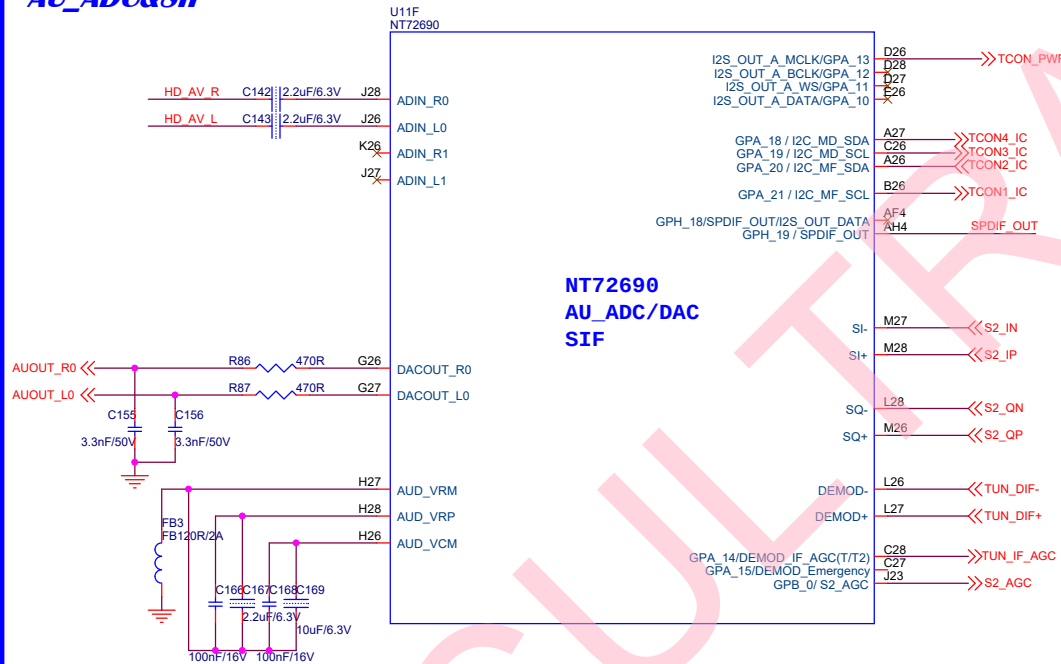
TV_ADC



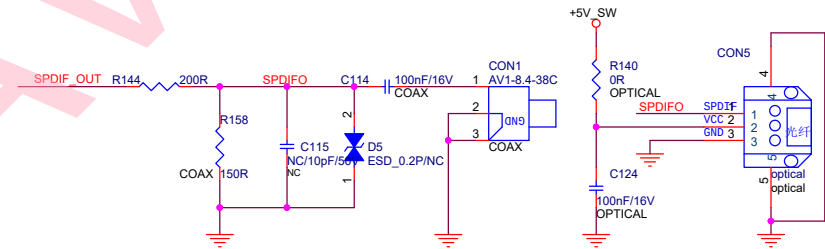
AV1_IN



AU_ADC&SIF

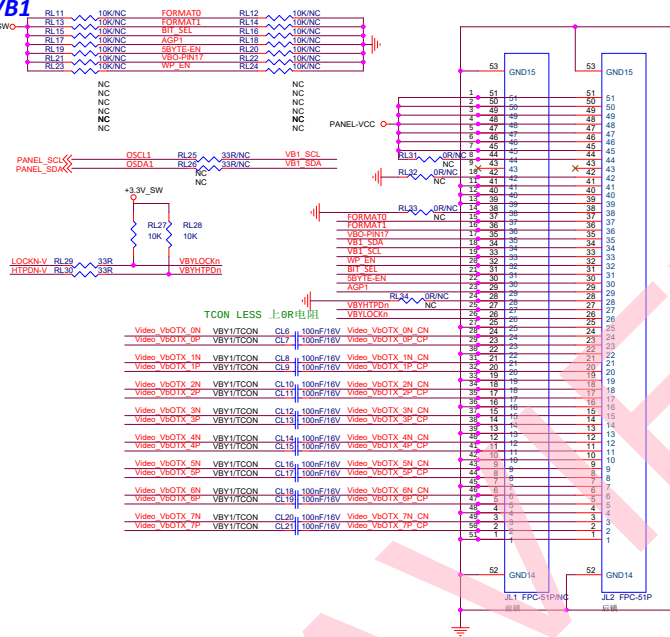


SPDIF OUT

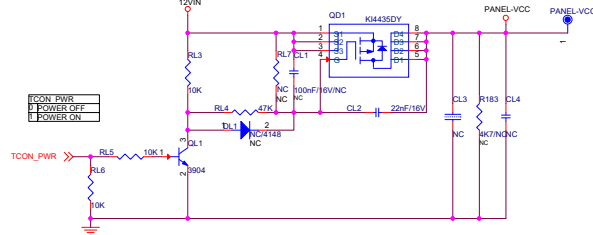


4K60Hz VB1

+3.3V_SW



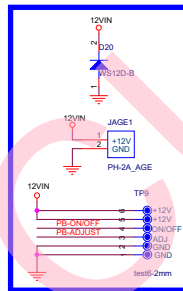
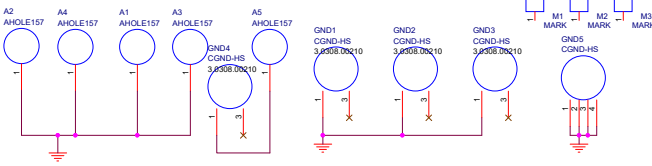
PANEL POWER



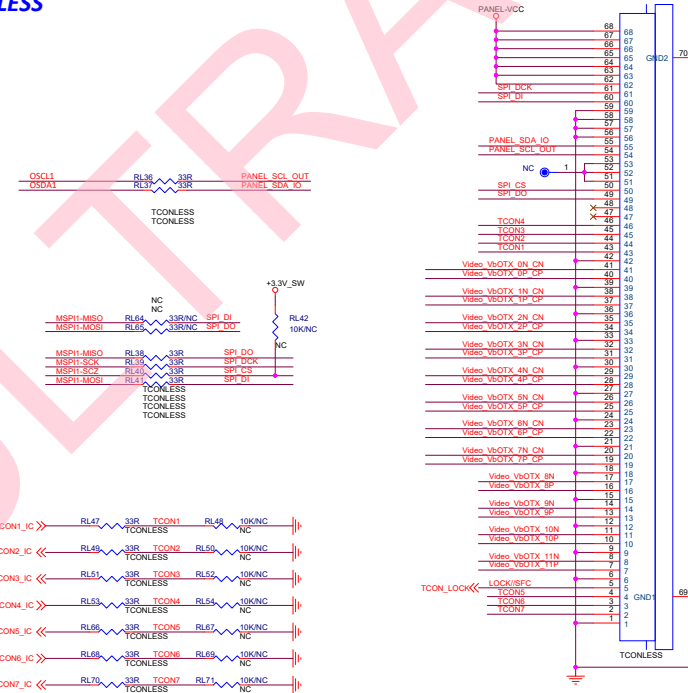
BackLight Controller

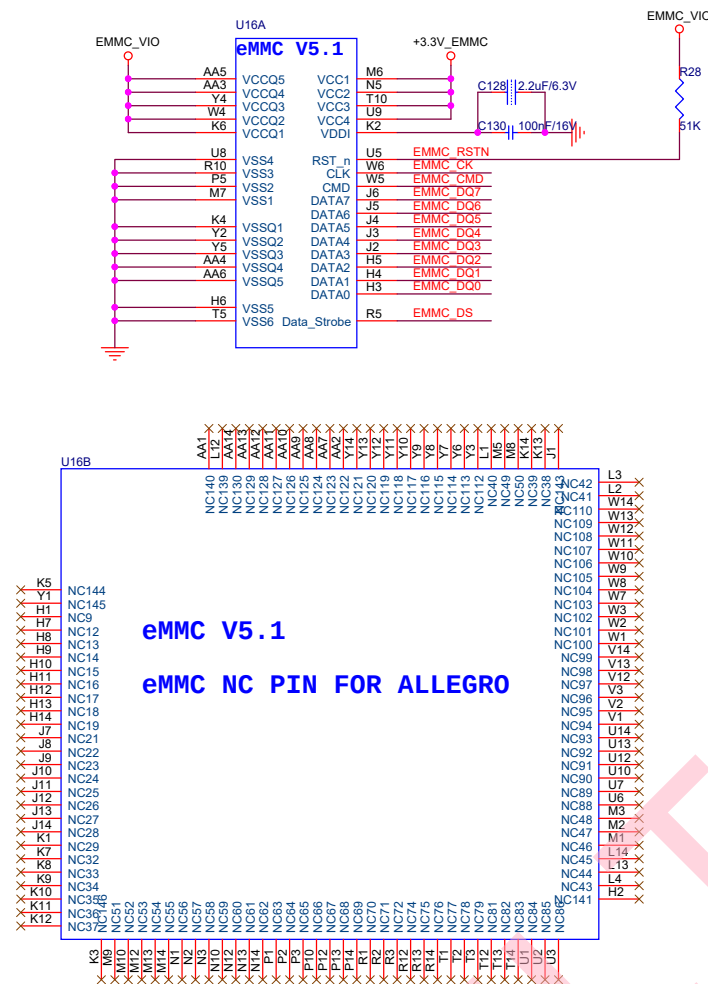


MARK & HOLE

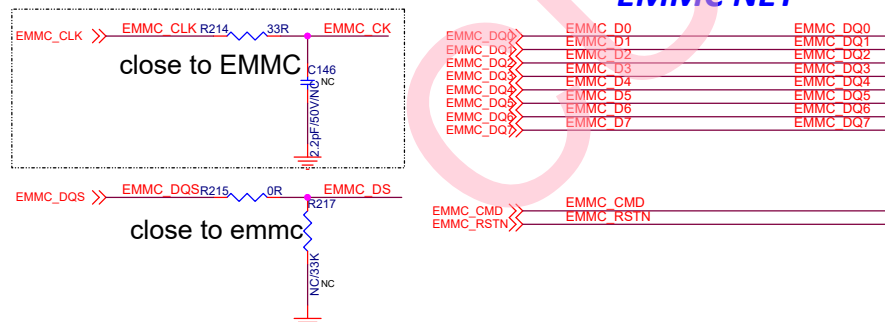


TCOON LESS

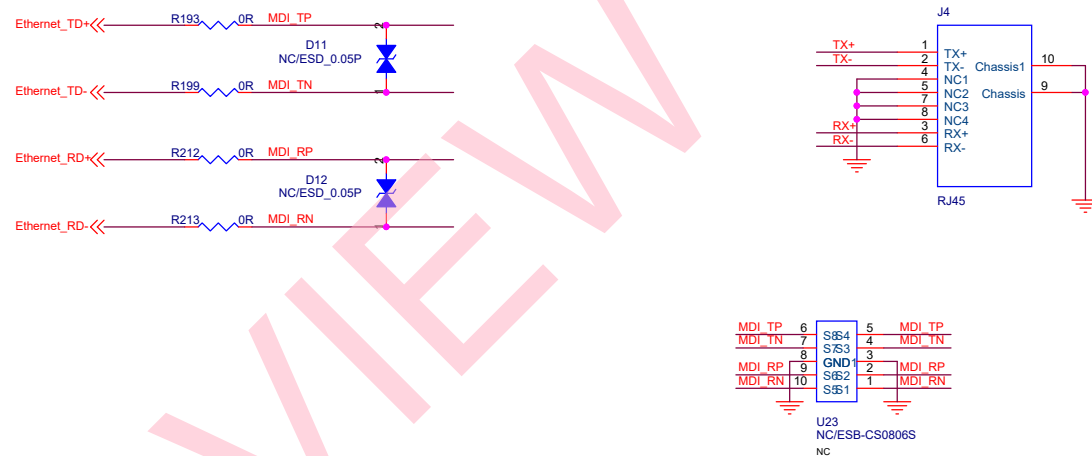


EMMC

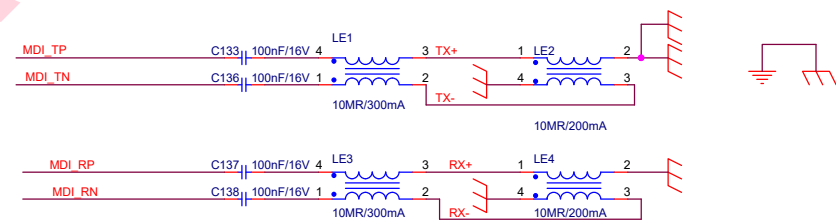
EMMC NET



Ethernet Connector



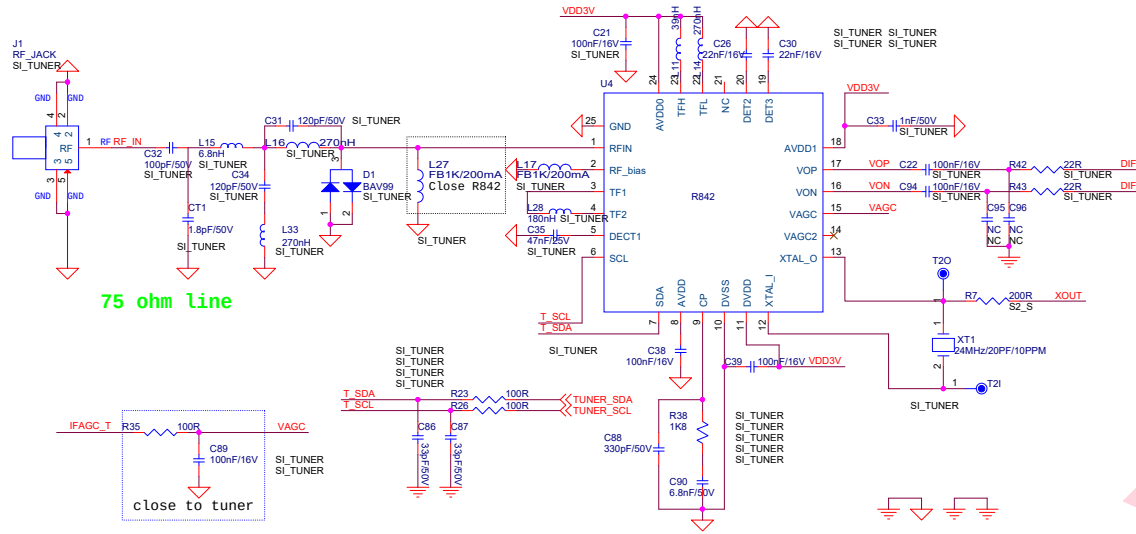
ENTHERNET 分立



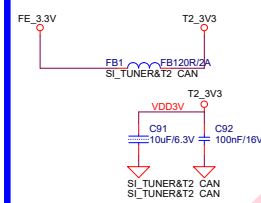
EMMC Power



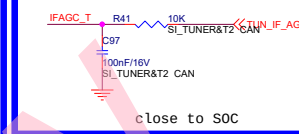
T/T2/C TUNER



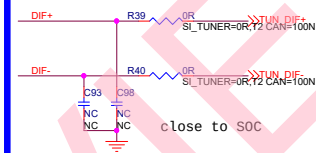
T2 Tuner Power



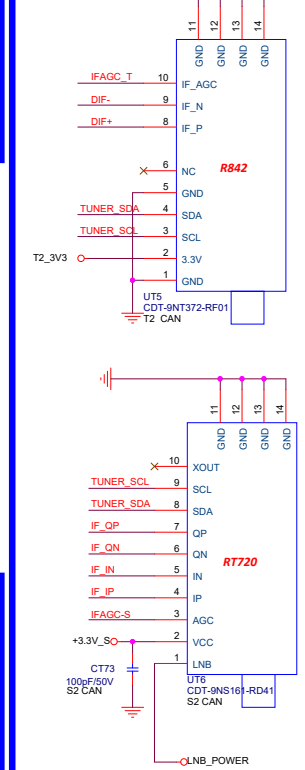
T2_AGC



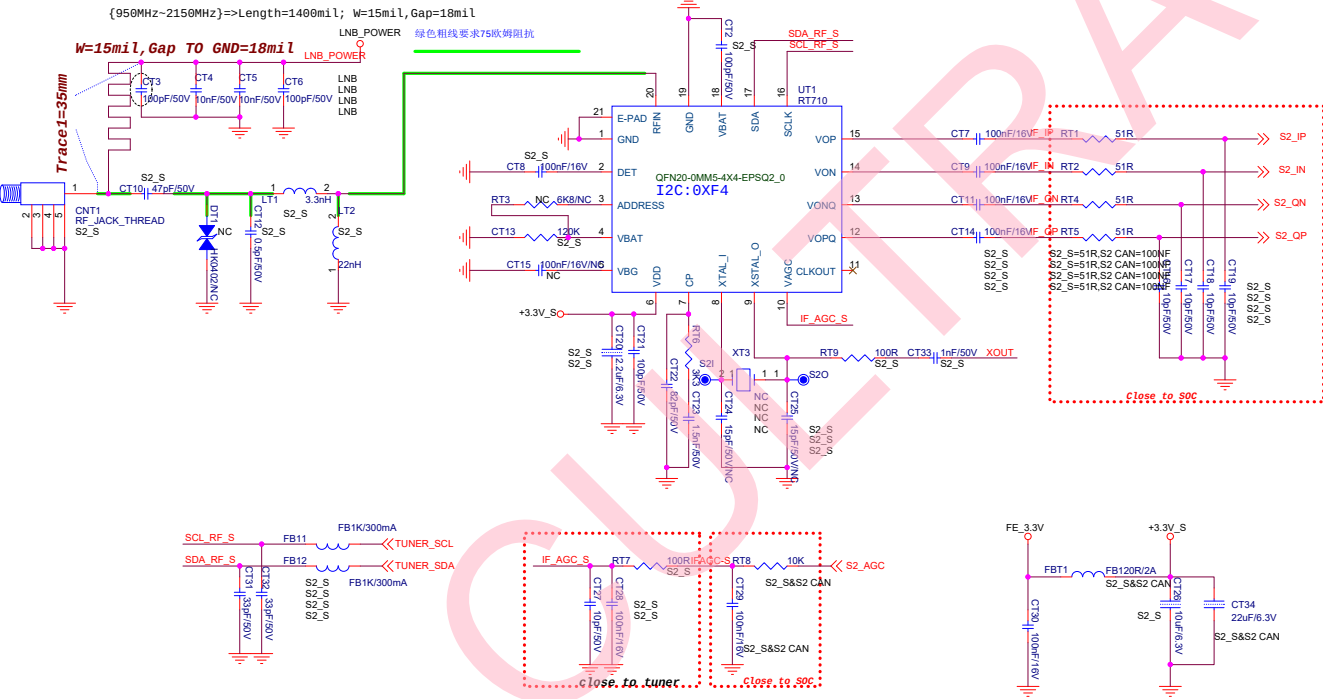
T2_IF



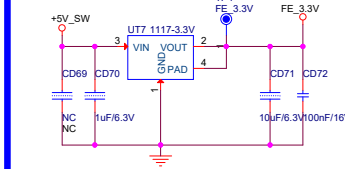
CAN TUNER



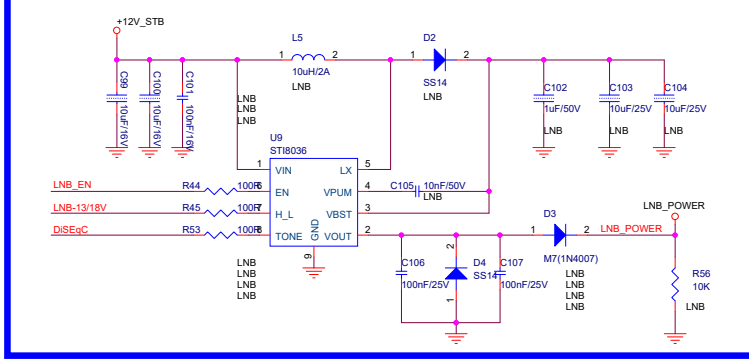
S2 TUNER



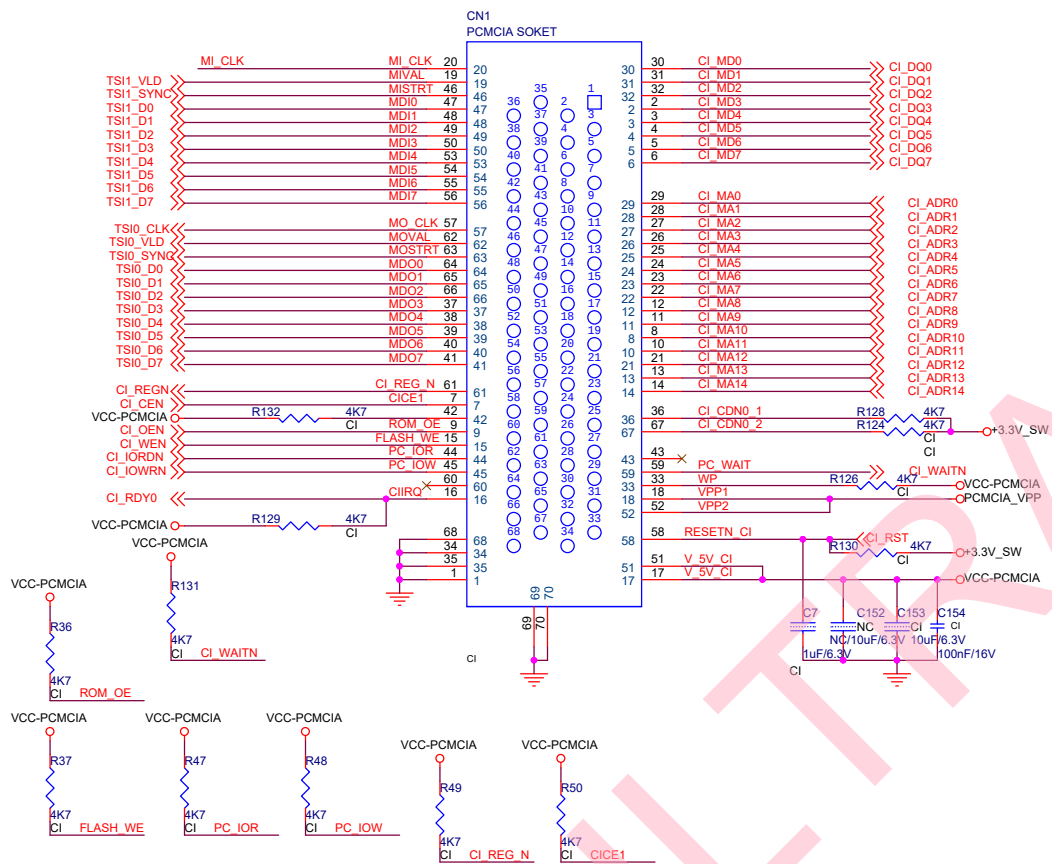
Tuner Power



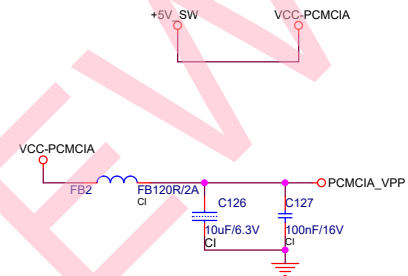
LNB POWER



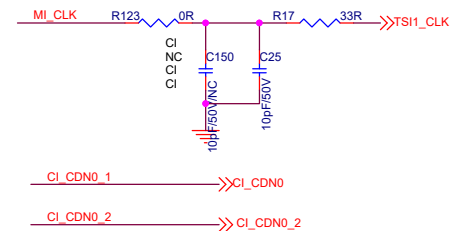
CI Socket



PCMCIA POWER



CLK



[illegible]

Headphone OP

The diagram shows a single-supply op-amp circuit for a headphone output. The op-amp, UA2 APA2172AOI-TRG, is configured with its non-inverting input (RINN) connected to AMP_RIN through RA14 and CA29, and its inverting input (RINP) connected to AMP_REF through RA17 and CA30. The output (ROUT) is connected to EAR_ROUT through RA15. The op-amp is powered by a +3.3V_SW supply, with decoupling capacitors CA33, CA34, CA35, and CA36. The op-amp is also connected to a +12V_STB supply through RA21 and CA32. The op-amp is configured with feedback resistors RA12, RA13, RA27, RA28, and RA15. The op-amp is configured with feedback resistors RA12, RA13, RA27, RA28, and RA15. The op-amp is configured with feedback resistors RA12, RA13, RA27, RA28, and RA15.

POWER

The diagram shows a power supply circuit. A red wire connects the +12V_STB pin to the AMP_POWER pin. A capacitor, labeled CA24 (470uF/16V), is connected in parallel with the AMP_POWER pin to ground (GND).

[illegible]

MUTE

AMP_MUTE
0 MUTE
1 NORMAL

AMP_MUTE >> RA10 4K7 AMP-EN

RA11 4K7

Ground

EARPHONE

Earphone Detect
H: Insert Earphone;
L: Pull Out Earphone;

PB-ADJUST >> PB-ADJUST
PB-ON/OFF >> PB-ON/OFF

